AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (currently amended) Storage control for ~~implementing~~ executing switch commands for access to storage cells for writing and reading data, which storage control receives control commands allocated to the data, contains for at least one storage type a command set with command sequences of individual switch commands to be processed in a predetermined succession and activated by the control commands,

which activates one after the other the switch commands of a command sequence corresponding to ~~the~~ a current control command, and

activates ~~the~~ a current switch command at a predetermined time later than the preceding switch command,

~~characterized in that~~

which activates the current switch command dependent on the previous switch command and the current control command, ~~the current switch command is activated, and~~

characterized in that

~~that~~ information items allocated to the storage cells are capable of being supplied to the storage control, which information items indicate the predetermined time mentioned~~.~~,

that the storage control contains command sets for several different storage types, and

that one command set can be determined by the information items.

2. (original) Storage control according to claim 1, characterized in that for every switch command a reference value (Zsoll) is stored in a first register (46).

3. (original) Storage control according to claim 2, characterized in that a counter (42) counts the impulses of an impulse series after the activating of the switch command.

4. (original) Storage control according to claim 3, characterized in that the counter reading (Z) is to be compared with the reference value (Zsoll), and that a first signal (READY) is created, if the counter reading (Z) is the same as the reference value (Z soll).

5. (original) Storage control according to claim 4, characterized in that the first signal (READY) is apprehended, and that on apprehending the first signal (READY) the next switch command is activated.

6. (original) Storage control according to claim 5, characterized by at least one switch command that is already activated before apprehending the first signal (READY).

7. (original) Storage control according to one of claims 2 to 6, characterized in that the reference values (Zsoll) for the switch commands are written in an installation process into the first register (46).

8. (original) Storage control according to one of the previous claims, characterized in that the first register (46) also contains a value for the time after which the storage content is to be refreshed.

9. (original) Storage control according to one of the previous claims, characterized by a device (52), which creates a second signal (NEW ACCESS), if the current control command belongs to a new command sequence.

10. (original) Storage control according to one of the previous claims, characterized in that operational control commands are created by the storage control for the processing of the individual switch commands of a command sequence in the predetermined succession.

11. (original) Storage control according to one of the previous claims, characterized in that the activating commands are stored in a second register (30).

12. (original) Storage control according to one of the previous claims, characterized in that the switch commands are stored in a third register (32).

13. (original) Storage controls according to claim 12, characterized in that the third register (32) is a write/read memory or a programmable read-only-memory, into which the switch commands are written in an initializing process.

14. (original) Storage control according to one of the previous claims, characterized in that a third signal (SAME LINE) is created, if the current command sequence relates to storage cells of the same line of the memory (18) as the previous command sequence.

15. (original) Storage control according to one of the previous claims, characterized in that the command set is determined for each respective storage type by means of information items allocated to the storage cells.

16. (original) Storage control according to one of the previous claims, characterized in that a fourth signal (DATAVALID) is created, when the writing or reading is concluded.

17. (original) Storage control according to claim 16, characterized in that the fourth signal (DATAVALID) is given back together with the source address for the access after the conclusion.

18. (original) Storage control according to claim 16 or 17, characterized in that a fifth signal is created if the current switch command is the first switch command of a new command sequence.

19. (original) Storage control according to claim 18, characterized in that the information items allocated to the storage cells also give the time, after which after activating the first switch command of each new command sequence, the writing or reading respectively is concluded.

20. (new) A memory controller system comprising:

a register for storing memory control commands and information regarding order and timing of the memory control commands, said commands and information being programmable into the register depending upon the type of memory being utilized;

an intermediate memory for storing a memory command that is currently being carried out;

a storage device for receiving access commands for reading and writing to a specified memory address, the access commands being issued by the host;

a switch unit for transmitting memory control commands as a function of the order of commands and timing information stored in the register, the contents of the intermediate memory and the access commands received from the host; and

wherein the host can communicate with different types of memory.

21. (new) The memory controller system of claim 20 further comprising a parallel access unit which identifies consecutive accesses to a common memory region, thereby allowing the switch unit to take advantage of a memory's burst mode when communicating with the common memory region.

22. (new) The memory controller system of claim 20 further comprising a reset signal, thereby allowing an ongoing memory command sequence to be interrupted.

23. (new) The memory controller system of claim 20 further comprising a timer which causes the switch unit to refresh contents of the memory storage system at pre-defined intervals.

24. (new) The memory controller system of claim 20, wherein the host is a computer microprocessor.

25. (new) The memory controller system of claim 20, wherein the host can communicate with different types of memory by programming the contents of the register.

26. (new) The memory controller system of claim 20, wherein the host can communicate with different types of memory by selecting the commands and information in the register to be used.